IN THE SPECIFICATION:

(1) The paragraph from page 2, line 20 to page 2, line 23 has been amended as follows:

It is another object of the present invention to provide a test language conversion method of converting test vectors in a STIL (Standard Test Interface Language) format into a target format with high efficiency and accuracy.

(2) The paragraph from page 5, line 25 to page 6, line 1 has been amended as follows:

In this patent specification, the inventor discloses some of the basic steps involved in conversion method from one cycle-based format to another cycle-based format. The inventor also presents some tricks that allow the conversion of STIL in an efficient manner. The conversions shown in this invention are based on an analysis of the data presented in STIL. As a sample target language, Test Description Language (TDL) ~~by~~ developed by Advantest Corporation, Tokyo, Japan, an assignee of this invention, is used for illustration purposes although the principles presented are general and thus equally applicable to other test languages.

(3) The paragraph from page 6, line 2 to page 6, line 9 has been amended as follows:

Figures 1-4 ~~showing~~ show examples of format in STIL for describing the digital test vectors. Figure 1 shows formats of signals and signal groups, Figure 2 shows formats of

timings of edges in each signal. Figure 3 shows an example of STIL format describing patterns of test vectors, and Figure 4 shows an example of STIL format describing the flow of patterns. Figure 5 is a diagram showing an example of format in TDL which is a target test language.

(4) The paragraph from page 7, line 1 to page 7, line 12 has been amended as follows:

Figure 6B is a functional representation of the test vector conversion of the present invention from the STIL test language to the TDL test language. ~~A~~ An STIL vector file 21 is a file storing STIL test vectors to be converted to TDL vectors through the conversion process of the present invention. Typically, the STIL test vectors in the STIL file 21 are derived from the design stage of semiconductor devices, i.e., CAE (Computer-Aided Engineering) environment or EDA (Electronics Design Automation) environment as a result of conducting logic simulation. The STIL test vectors are decomposed into constituent events and stored in a decomposed event file 24.

(5) The paragraph from page 7, line 13 to page 7, line 19 has been amended as follows:

As noted above, TDL is a test language developed by Advantest Corporation, the assignee of the present invention, to establish a logic test pattern (LPAT) file. The format of TDL is stored in a TDL wavekind file 22. Each waveform

defined in the target test language ~~**TDL,**~~ TDL is converted to a corresponding template having a set of components. Such templates of waveforms are stored in a template file 25.

(6) The paragraph from page 7, line 34 to page 8, line 16 has been amended as follows:

01 {'400ns' D/U;} => NRZ; T1=400ns; T2=400ns

where the ~~**STIL**~~ STIL construct 01 {'400ns' D/U;} in the left means that the character '0' specifies a falling edge (D) at 400ns while the character '1' specifies a rising edge (U) at 400ns. This ~~**STIL**~~ STIL representation corresponds to the waveforms shown in the upper part of Figure 8 and to a non-return zero (NRZ) waveform defined in TDL. In Figure 8, the waveform of character '0' shows the shaded portion from the start edge of a test cycle to the falling edge T1 ~~**(400ns**~~ at 400ns from the start edge. The shaded portion means that the logic state in this area is undefined. Thus, the character '0' defines the falling edge T1 at 400ns from the start of the test cycle whatever the current logic status is. Similarly, the waveform of the character '1' defines the ~~**falling**~~ rising edge T1 at 400ns from the start of the test cycle whatever the current logic status is. As noted above, this example of STIL construct corresponds to the NRZ waveform of TDL.